What is Claimed is

1. A fabrication method of a semiconductor integrated circuit device comprising the steps of:

(a) preparing a polishing slurry in the stable particle dispersion state;

(b) diluting said polishing slurry with a water solution, which has deionized water as a main component; and

(c) supplying the polishing slurry on the surface of the wafer undergoing the mass-production process immediately after being diluted with said water solution to apply the chemical-mechanical polishing method.

2. A fabrication method of a semiconductor integrated circuit device according to Claim 1, wherein said polishing slurry in the stable particle dispersion state contains 11 - 15 weight % silica.

3. A fabrication method of a semiconductor integrated circuit device according to Claim 2, wherein said polishing slurry in the stable particle dispersion state contains 11 - 13 weight % silica.

4. A fabrication method of a semiconductor integrated circuit device according to Claim 2, wherein said polishing slurry in the stable particle dispersion state contains 12-weight % silica.

5. A fabrication method of a semiconductor integrated circuit device according to Claim 1, wherein a mixture ratio of said

polishing slurry and said water solution is 1 (polishing slurry) : 1 - 1.2 (water solution).

6. A fabrication method of a semiconductor integrated circuit device according to Claim 1, wherein after said polishing slurry is diluted with said water solution, it is supplied on the surface of said wafer to be polished within two hours.

7. A fabrication method of a semiconductor integrated circuit device according to Claim 6, wherein after said polishing slurry is diluted with said water solution, it is supplied on the surface of said wafer to be polished within ten minutes.

8. A fabrication method of a semiconductor integrated circuit device according to Claim 7, wherein after said polishing slurry is diluted with said water solution, it is supplied on the surface of said wafer to be polished within 10 - 15 seconds.

9. A fabrication method of a semiconductor integrated circuit device according to Claim 2, wherein the pH value of said polishing slurry in the stable particle dispersion state is 10.5 - 11.5.

10. A fabrication method of a semiconductor integrated circuit device according to Claim 1, wherein said polishing slurry in the stable particle dispersion state is used after it has been left at rest until the concentration of coagulated particles with a diameter of 1μm or more contained in it becomes 200,000/0.5cc or less.

11. A fabrication method of a semiconductor integrated circuit

device according to Claim 10, wherein said polishing slurry in the stable particle dispersion state is used after it has been left at rest until the concentration of coagulated particles with a diameter of 1μm contained in it becomes 50,000/0.5cc or less.

12. A fabrication method of a semiconductor integrated circuit device according to Claim 11, wherein said polishing slurry in the stable particle dispersion state is used after it has been left at rest until the concentration of coagulated particles with a diameter of 1μm or more contained in it becomes 20,000/0.5cc or less.

13. A fabrication method of a semiconductor integrated circuit device according to Claim 1, wherein said polishing slurry in the stable particle dispersion state is used after it has been left at rest for 30 days or more.

14. A fabrication method of a semiconductor integrated circuit device according to Claim 13, wherein said polishing slurry in the stable particle dispersion state is used after it has been left at rest for 40 days or more.

15. A fabrication method of a semiconductor integrated circuit device according to Claim 14, wherein said polishing slurry in the stable particle dispersion state is used after it has been left at rest for 45 days or more.

16. A fabrication method of a semiconductor integrated circuit device comprising the steps of:

(a) preparing a polishing slurry containing 11 - 15 weight % of silica;

(b) diluting said polishing slurry with a water solution or chemical solution, which has deionized water as a main component; and

(c) supplying the polishing slurry on the primary surface of the wafer undergoing the mass-production process immediately after being diluted with said water solution or the said chemical solution, thereby applying the chemical-mechanical polishing method to form an insulating groove smoothed by polishing on the primary surface of said wafer.

17. A fabrication method of a semiconductor integrated circuit device according to Claim 16, wherein a mixture ratio of said polishing slurry and said water solution or said chemical solution is 1 (polishing slurry) : 1 - 1.2 (water or chemical solution).

18. A fabrication method of a semiconductor integrated circuit device according to Claim 16, wherein after said polishing slurry is diluted with said water solution or said chemical solution, it is supplied on the primary surface of said wafer to be polished within two hours.

19. A fabrication method of a semiconductor integrated circuit device according to Claim 18, wherein after said polishing slurry is diluted with said water solution or said chemical solution, it is supplied on the primary surface of said wafer

to be polished within 10 minutes.

20. A fabrication method of a semiconductor integrated circuit device according to Claim 19, wherein after said polishing slurry is diluted with said water solution or said chemical solution, it is supplied on the primary surface of said wafer to be polished within 10 - 15 seconds.

21. A fabrication method of a semiconductor integrated circuit device according to Claim 16, wherein the concentration of coagulated silica particles with a diameter of 1μm or more contained in said polishing slurry prepared in said step (a) is 200,000/0.5cc or less.

22. A fabrication method of a semiconductor integrated circuit device according to Claim 16, wherein said polishing slurry prepared in said step (a) has been left at rest for 30 days or more beforehand.

23. A fabrication method of a semiconductor integrated circuit device according to Claim 16, wherein said polishing slurry prepared in said step (a) contains 11 - 13 weight % silica.

24. A fabrication method of a semiconductor integrated circuit device according to Claim 23, wherein said polishing slurry prepared in said step (a) contains 12-weight % silica.

25. A fabrication method of a semiconductor integrated circuit device comprising the steps of:

(a) forming a groove in a element-isolating region of the primary surface of a wafer by etching the element-isolating

region of primary surface of said wafer using a oxidation-resistant insulating film formed over the primary surface of said wafer as a mask;

(b) forming a silicone oxide insulating film over the primary surface of said wafer including the inside of said groove;

(c) diluting the polishing slurry containing 11 - 15 weight % of silica with deionized water; and

(d) supplying the polishing slurry on the primary surface of said wafer, for which step (b) has been finished, immediately after being diluted with said water solution and chemically-mechanically polishing said silicone oxide insulating film using said oxidation-resistant insulating film as a stopper to selectively leave said silicone insulating film inside said groove, forming the insulating, isolating film smoothed by polishing in said element isolating region.

26. A fabrication method of a semiconductor integrated circuit device according to Claim 25, wherein after said polishing slurry is diluted with said water solution, it is supplied on the primary surface of said wafer within two hours.

27. A fabrication method of a semiconductor integrated circuit device according to Claim 26, wherein after said polishing slurry is diluted with said water solution, it is supplied on the primary surface of said wafer within ten minutes.

28. A fabrication method of a semiconductor integrated circuit device according to Claim 27, wherein after said polishing

slurry is diluted with said water solution, it is supplied on the primary surface of said wafer within 10 - 15 seconds.

29. A fabrication method of a semiconductor integrated circuit device comprising the steps of:

(a) preparing the polishing slurry containing 11 - 15 weight % of silica; and

(b) supplying said polishing slurry and said water solution made mainly of deionized water on the primary surface of the wafer undergoing the mass-production process to apply chemical-mechanical polishing.

30. A fabrication method of a semiconductor integrated circuit device according to Claim 29, wherein a mixture ratio of said polishing slurry and said water solution is 1 (polishing slurry) : 1 - 1.2 (water solution).

31. A fabrication method of a semiconductor integrated circuit device according to Claim 29, wherein the concentration of said coagulated silica particles with a diameter of 1μm contained in said polishing slurry is 200,000/0.5cc or less.

32. A fabrication method of a semiconductor integrated circuit device according to Claim 29, wherein said polishing slurry has been left at rest for 30 days or more beforehand.

33. A fabrication method of a semiconductor integrated circuit device according to Claim 29, wherein said step (b) is the step of forming the insulating film isolating groove smoothed by polishing on the primary surface of said wafer.

34. A fabrication method of a semiconductor integrated circuit device according to Claim 29, wherein said polishing slurry prepared in said step (a) contains 11 - 13 weight % silica.

35. A fabrication method of a semiconductor integrated circuit device according to Claim 34, wherein said polishing slurry prepared in said step (a) contains 12-weight % silica.